

# SPACEWIRE TEST AND DEMONSTRATION UTILISING THE INTEGRATED PAYLOAD PROCESSING MODULE

**Session: Missions and Applications**

**Short Paper**

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## **ABSTRACT**

The Integrated Payload Processing Module (IPPM), developed by Aurelia Microelectronics under the frame of the European Space Agency Technology Research Programme, is a versatile payload computer board featuring the AT697E Leon2 CPU and the FPGA implementation of the SpaceWire Router 10X. The IPPM features in addition 262MB of on-board memory which is accessible via the Remote Memory Access Protocol (RMAP), MIL-STD-1553 and CAN bus interfaces, and general purpose I/O. These key features are utilised to establish an on-board data handling demonstration platform. The demonstration platform is based on 3 IPPM boards and complementary demonstration equipment play the role of Mass Memory, and a TM/TC and Display unit serving as a Ground Control Unit (GCU). The overall demonstration set-up aims to resemble a simplified onboard data handling system which communicates with a simulated ground station for telemetry and science data up/down links. Each of the three IPPM boards will have a dedicated role as an onboard data handling unit. One IPPM board will act as an Instrument Unit (IU), while the other two boards acts as Processing Module for the Payload Data handling Unit (PDHU) and as Satellite Management Unit (SMU), respectively. Each IPPM board will be running RTEMS as Operating System (OS) as well as applications that support a subset of services in accordance with the Packet Utilisation Standard (ECSS-E-40-71A). The above described demonstration baseline will be exploited to perform experiments in the domains of; PnP, Command & Control over SpaceWire, and also establish and demonstrate best practices for current and near-coming use of SpW links and routers; e.g. network topology, redundancy schemes, SpaceWire Networking Protocols etc.