SoCWire: A SpaceWire inspired fault tolerant Network-On-Chip for Reconfigurable System-on-Chip Designs in Space Applications

Spacewire network and protocols

Short Paper

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Abstract

Configurable System-on-Chip (SoC) solutions based on state-of-the art FPGA have successfully demonstrated flexibility and reliability for scientific Data Processing Units (DPUs) like the Venus Monitoring Camera (VMC) on Venus Express. Future high end payload applications (e.g. Solar Orbiter) demand high-performance on-board processing because of the discrepancy between extreme high data volume and low downlink channel capacity [1]. Furthermore, in-flight reconfiguration ability enhances the system with reprogrammable hardware and thus a maintenance and improvement potential. For an in-flight update of a processing module the once on ground achieved qualification and reliability of the total system has to be maintained. The update process or an SEU in the processing module logic could stop the system. Therefore the processing module needs to be isolated from the host system physically and logically. Partial reconfiguration permits to define Partial Reconfigurable Areas (PR-Areas) in the FPGA for Partial Reconfigurable Modules (PRMs) which are physically isolated from the surrounded configuration memory space. Therefore we subdivided the system into (1) a static area, which remains unchanged during the whole mission and comprises all critical functions and interfaces (e.g. processor, interfaces to spacecraft) and (2) PR-Areas which can be updated during flight. DPUs are usually based on bus structures (e.g. AMBA, Wishbone) but the classical instrument DPU functional architecture is a macro-pipeline system with pre- and post-processing steps and high data rate point-to-point communication. To realize this architecture in a bus structure, multi master and bus arbitration capabilities are needed. Furthermore an SEU in the PRM bus interface logic could stop the system. Therefore a failure tolerant bus structure, which usually needs high effort, is necessary to guarantee data integrity. To overcome the limitation of a bus structure we considered a networked architecture with a Network-on-Chip (NoC) approach *System-on-Chip Wire (SoCWire)* providing a reconfigurable point-to-point communication architecture and supporting an adaptive macro-pipeline structure. An example SoCWire system is shown in Figure 1.

SoCWire is based on the SpaceWire interface standard. SpaceWire is a well established standard [2] and proven interface for space application. It is a serial link interface, uses data strobe encoding and achieves data rates up to 400 Mb/s. The

performance of the interface depends on skew, jitter and the implemented technology. Since we are in a complete on-chip environment we have modified the SpaceWire interface to a 10 bit (1 parity bit , 1 data-control flag bit, 8 data bits) parallel data interface. The advantage of this parallel data transfer interface is that we can achieve significantly higher data rates in comparison to SpaceWire of e.g. 800 Mbit/s @ 100 Mhz. Additionally, we have implemented a scalable data word width (8-128 bit) to achieve even higher data rates, e.g. for 32bit data word width @100 Mhz → 3.2 Gbit/s. The SpaceWire standard flow control mechanisms are still supported. Another benefit is the hot-plug ability of the SoCWire architecture which is suitable for dynamic reconfigurable systems. SoCWire isolates the PRMs logically from the host system. With SoCWire and PR-Areas the system qualification can be guaranteed with additional module self-testing features (test vector, timing constraint test functions).

In this paper we will present our NoC approach SoCWire and outline its suitability for partial reconfigurable systems in space applications.

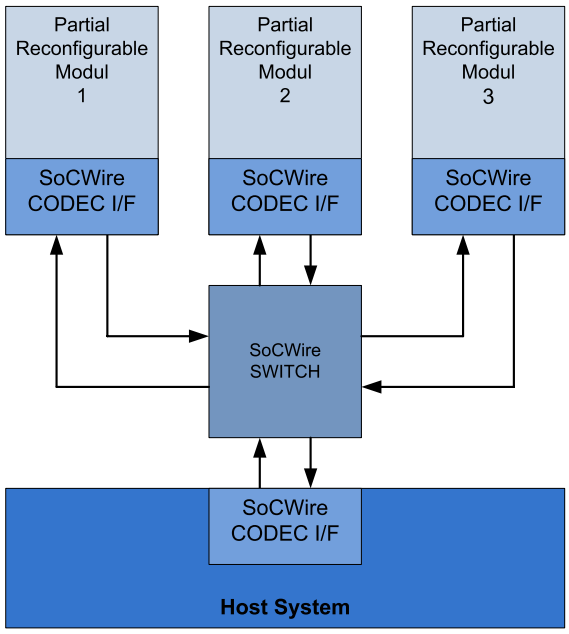

Figure1: SoCWire system

References:

[1] B. Osterloh, H. Michalik, B. Fiethe, K. Kotarowski, *ADVANCED SYSTEM-ON-CHIP DESIGN WITH IN-FLIGHT RECONFIGURABLE PROCESSING CORES FOR SPACE APPLICATIONS,* DASIA 2008

[2] ECSS, *Space Engineering: SpaceWire–Links, nodes, routers, and networks*, ESA-ESTEC, Noordwijk Netherlands, January 2003, ECSS-E-50-12A