A CPU MODULE FOR A SPACECRAFT CONTROLLER WITH HIGH THROUGHPUT SPACEWIRE INTERFACES

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Short Paper

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ABSTRACT

We have developed the CPU module for a spacecraft controller with high throughput SpaceWire interfaces. This CPU module is a main module of the spacecraft controller which executes AOC(Attitude and Orbit Control) and DH(Data Handling) processing.

The amount of data from payload subsystems has been increasing in recent spacecrafts, such as earth observing spacecrafts. Therefore we selected SpaceWire for its high data transfer rate. To accelerate data transfer throughput without requiring excessive CPU resources, we have developed a SpaceWire controller with (1) a DMA controller to reduce CPU's I/O operations, (2) a PCI bus bridge with master capability which enables data transfer between CPU local memories and SpaceWire interfaces, (3) two sets of control registers with an auto flip function for each DMA channel which continues data transfer even when the CPU is setting up the next DMA transfer.

The CPU module is composed of the HR5000 CPU which is developed by JAXA, memories and an FPGA. The SpaceWire interfaces are implemented on an Anti-Fuse FPGA and connected to the CPU via PCI bus. This CPU module is a part of the SCU (Spacecraft Control Unit) which is integrated with Sensor Interface modules, I/O modules and Data Recorder modules.

We have made a functional model of the CPU module and evaluated the performance of data transfer. This paper shows the architecture of the CPU module and its evaluation results.