CRUCIAL SPACEWIRE ELEMENTS IN RASTA

Session: SpaceWire Equipment and Software

Short Paper

Sandi Habinc, Jiri Gaisler

Gaisler Research, Första Långgatan 19, SE-413 27 Göteborg, Sweden

Claudio Monteleone, Chris Taylor

European Space Agency, Keplerlaan 1, P.O. Box 299, NL-2200 AG Noordwijk, The Netherlands

E-mail: sandi@gaisler.com, jiri@gaisler.com, claudio.monteleone@esa.int, chris.taylor@esa.int

ABSTRACT

The RASTA (Reference Avionics System Test-bench Activity) was initiated by the European Space Agency (ESA) to provide a single development platform to reduce the number of prototyping environments established in technology developments.

The RASTA objectives are to allow the developed technology items to be validated and demonstrated in a flight representative prototype environment, to support mission and spacecraft design and on-board software validation through the project life-cycle by means of a coherent development platform, to maximize reuse of the existing avionics technologies and to be scalable and flexible.

The main communication interface used in RASTA is SpaceWire network [1]. Some of the crucial elements of the RASTA initiative are based on the GRSPW SpaceWire Link Codec IP core [5] developed by Gaisler Research, Sweden. The IP core has been included in many of the FPGA and ASIC implementations that are used in the RASTA boards.

1 OVERVIEW

The RASTA development platform has been developed for ESA to provide the means to demonstrate functional and performance requirements of satellite on-board systems and subsystems. A crucial part of the RASTA development platform is the SpaceWire network and the elements implementing it. The key elements implementing the SpaceWire network are the various RASTA boards harbouring ASIC or FPGA components featuring SpaceWire links.

A variety of boards have been developed to support the design of complex avionics and payload management systems. These boards carry components with SpaceWire interfaces from a number of different manufactures. For example, boards have been developed to support the Aeroflex UT699 device, the Atmel AT7913E (SpaceWire-RTC) ASSP and the LEON3FT-RTAX Actel FPGA based processors.

Other boards are also compatible with the RASTA concept, such as the SpaceWire router boards from Aeroflex and Star-Dundee. Generic FPGA boards targeting Xilinx and Actel devices are used to implement system-on-a-chip configuration.

To be representative, the RASTA development platform is based on flight compatible hardware and software. This is supplemented by the addition of a workstation hosting the cross-development and debugging environment for software development. The two together provide an "easy to use" facility that allows developers to perform tests and validation, at system level, in a highly representative environment.

2 PROCESSOR BOARDS

The main building blocks of the RASTA development platform are the processor boards. The processor boards contain basic memory and debug interfaces, such as the LEON2/3 Debug Link UART and JTAG. The boards also contain an Ethernet 10/100 Mbit/s MAC and PHY, which can be used with RTEMS or VxWorks Workbench.

Processing can also be provided by means of FPGA devices, with the LEON3 SPARC processor [6] pre-programmed into either an Actel or a Xilinx FPGA. The latter allows for prototyping of processor systems with novel features such as multiple processor cores or a memory management unit.

All processor boards can also be extended with accessory boards providing common interfaces such as RS-232 UART interfaces.

3 INTERFACE BOARDS

For interfaces other than a simple UART, the processor boards can communicate via the cPCI backplane to interface boards implementing dedicated communication protocols. Each interface board implements a PCI Initiator and Target interfaces to allow efficient communication with the processor board.

The initiator capability allows the interface board to implement direct memory access (DMA), off-loading the processor from repetitive task such as periodic data movement. This concept has been proven with the Advanced Data and Power Management System (ADPMS) on the PROBA-2 spacecraft.

The PCI interface has the following capabilities:
- 32-bit bus width, 33 MHz (133 MByte/s)
- 32-bit DMA bus master (133 MByte/s)

In the future, the cPCI back-plane interface will be replaced with an active SpaceWire backplane using SpaceWire routers. For now, the SpaceWire communication is done via front-panel connectors.

The interface boards implement the various communication protocols. The following communication protocols have been implemented so far:
- SpaceWire with Remote Access Memory Protocol (RMAP)
- Redundant Mil-Std-1553B bus
- Controller Area Network (CAN) 2.0B
- 10/100 Mbps Ethernet

- ECSS/CCSDS Telemetry, with PacketWire etc.
- ECSS/CCSDS Telecommand, with PacketWire etc.
- CCSDS Time Management with TimeWire
- General Purpose Input Output (GPIO)

The key SpaceWire interface has the following capabilities:
- 200 Mbps maximum rate, full duplex, DMA capability
- Remote Access Memory Protocol (RMAP) [2]
- MDM connectors with LVDS electrical levels

The CCSDS telemetry and telecommand interface has the following capabilities:
- Two different telecommand decoders
- Two different telemetry encoders, with support up to 8 Virtual Channels
- Dedicated PacketWire and SpaceWire interfaces

Each interface board also implements a memory controller interfacing the following memory. The memory can be used as safeguard memory required for the processor board to communicate with the remaining representative flight data systems in the RASTA architecture.

One or more of the above interfaces can be implemented on the same interface board. The internal RASTA interface board FPGA design is based on the de-facto standard AMBA Advanced High-speed Bus (AHB) [3], to which the high-bandwidth units are connected. Low-bandwidth units are connected to the AMBA Advanced Peripheral Bus (APB), which is accessed through an AHB to APB bridge.

4 FUTURE BOARDS

The RASTA development platform has been developed to take into account future development boards, covering upcoming processor devices and for example SpaceWire router ASICs.

To mention a few examples, the UT699 (Aeroflex) 6U cPCI board features the LEON3-FT processor, the UT200SpW16RTR-EVB (Aeroflex) 6U cPCI evaluation board features a 16-port SpaceWire router, and the SpaceWire-RTC (AT7913E Atmel) ASIC development suite features a 6U cPCI ASIC board.

Other interfaces can also be developed, such as I2C, SPI, USB and Gigabit Ethernet, by using IP cores from the Gaisler Research VHDL IP core library GRLIB [4].

5 INTEGRATION

To allow for simple hardware integration, all boards used in the RASTA development platform are compliant with the cPCI standard. The boards are pre-assembled during system integration and verification using commercial cPCI crates, either 3U or 6U depending on what boards are required. Each RASTA system is shipped ready to use in a cPCI crate together with cabling, documentation and demonstration software.

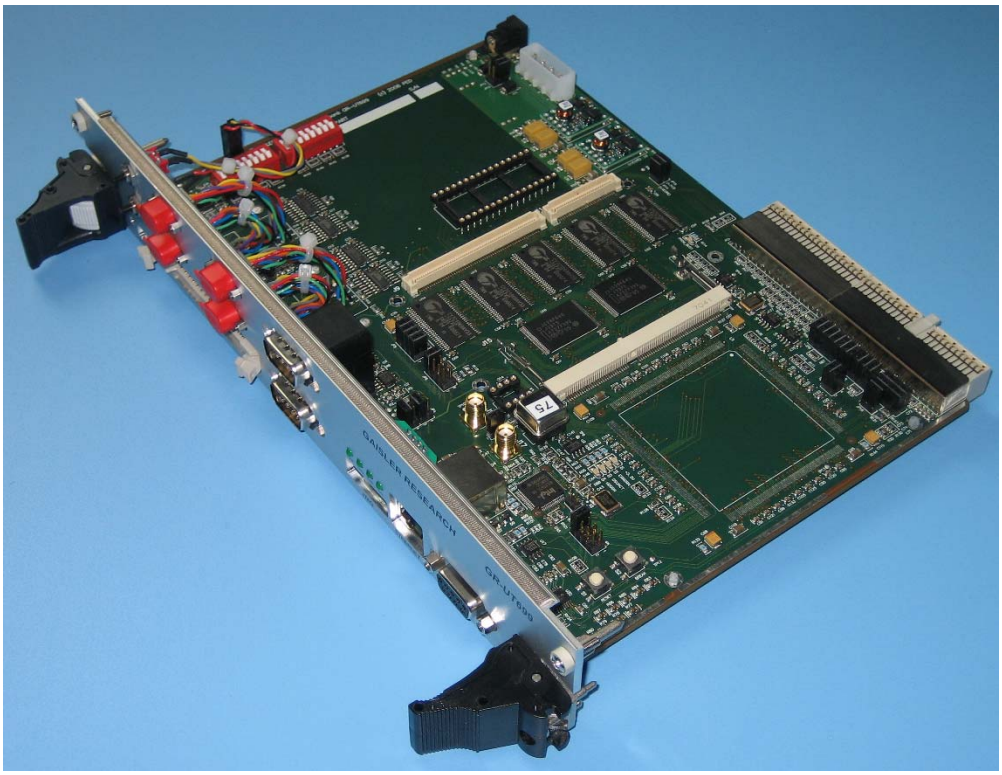

Figure 1 – Example of a 6U high UT699 LEON3FT processor board that fits in a RASTA system

6 CONCLUSION

The critical SpaceWire elements in the RASTA initiative have been largely based on the GRSPW SpaceWire Link Codec IP core. The core has the capability to directly interface to the AMBA AHB and APB on-chip buses by means of DMA capability. The core also implements the complete RMAP communication protocol directly in hardware. The use of RMAP in combination with on-chip or off-chip processors provides the possibility for remote software debugging over SpaceWire.

7 REFERENCES

1. "SpaceWire standard - Links, nodes, routers and networks", ECSS-E-ST-50-12C, 31 July 2008

2. "SpaceWire protocols", ECSS-E-ST-50-11C, July 2008

3. "AMBA Specification, Rev 2.0, ARM IHI 0011A, 13 May 1999, Issue A, first release, ARM Limited

4. "GRLIB IP Library User's Manual", Gaisler Research, www.aeroflex.com/gaisler

5. "GRLIB IP Core User's Manual", Gaisler Research, www.aeroflex.com/gaisler

6. "The SPARC Architecture Manual", Version 8, Revision SAV080SI9308, SPARC International Inc.