DESIGNING SPACE CUBE 2 WITH ELEGANT FRAMEWORK

Session: SpaceWire test and verification

Short Paper

Hiroki Hihara

NEC TOSHIBA Space Systems, Ltd., 10, Nisshin-cho 1-chome, Fuchu, Tokyo, Japan

Shuichi Moriyama, and Tatsuya Takezawa

NEC Soft, Ltd., 2-22 Wakaba-cho, Kashiwazaki, Niigata, Japan

Yuji Nishihara

JAXA's Engineering Digital Innovation Center, Japan Aerospace Exploration Agency (JAXA), Tsukuba Space Center, Sengen 2-1-1, Tsukuba, Ibaraki, 305-8505, Japan

Masaharu Nomachi

Laboratory of Nuclear Studies, Graduate School of Science, Osaka University,

1-1 Machikaneyama, Toyonaka, Osaka 560-0043

Tadayuki Takahashi, and Takeshi Takashima

Department of High Energy Astrophysics, Institute of Space and Astronautical Science (ISAS), Japan Aerospace Exploration Agency (JAXA), 3-1-1 Yoshinodai, Sagamihara,Kanagawa 229-8510, Japan

E-mail: hihara.hiroki@ntspace.jp, moriyama@mxp.nes.nec.co.jp, takezawa@mxa.nes.nec.co.jp, nishihara.yuuji@jaxa.jp, nomachi@lns.sci.osaka-u.ac.jp, takahasi@astro.isas.jaxa.jp, ttakeshi@stp.isas.jaxa.jp

ABSTRACT

Faced with growing demands for function and performance of satellite onboard equipments with maintaining reliability, Japan Aerospace Exploration Agency (JAXA) has developed ELEGANT (Electric Design Guidance Tool for Space Use), a complete C-language based environment for electronic system-level (ESL) design of space and satellite electronics. Space Cube 2 is not only the first SpaceWire based satellite onboard system controller in Japan but also the first real application of ELEGANT framework. ELEGANT provides a seamless tool chain for modelling verification and synthesis from top-level specification down to embedded Hardware/Software implementation. Performance trade-off associated with candidate system architectures has been accomplished early in the system design phase.

1 INTRODUCTION

Space Cube 2 (Figure 1) is the first SpaceWire based satellite onboard system controller in Japan [1] as well as the first real application of ELEGANT (Electric Design Guidance Tool for Space Use), which is developed by Japan Aerospace

Exploration Agency (JAXA) [2]. ELEGANT has the capability of top down design using hardware and software collaborating design methodology.

Figure 1(a): Space Cube 2 (Flight Model)

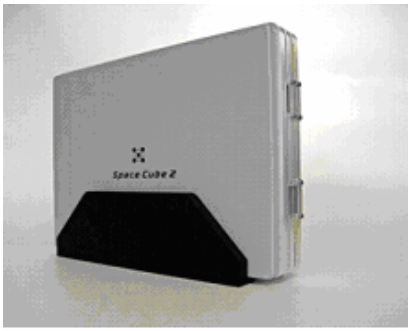


Figure 1(b): Space Cube 2/C (Development Platform)

The system level specification is modelled as behaviours and channels, which is described in SpecC language, as standardized by the SpecC Technology Open Consortium (STOC) [3], at the first step in ELEGANT design flow. The specification model can be verified by simulation subsystem within the specification model simulator. After the specification is verified, designers can evaluate and select among candidate architectures assisted by the architecture exploration tools. Evaluation based on processing speed, software execution steps and hardware scale in accordance with several hardware-software partitioning is possible. In consequence, designers can select the most suitable architecture for their project demands. Once the architecture is fixed, the behaviour description written in SpecC is synthesized into HDL (hardware description language) directly with behaviour synthesis tool.

2 ELEGANT

2.1 ELEGANT ENVIRONMENT

ELEGANT (Figure 2) provides an environment for top-down electronic system-level (ESL) design. Under JAXA's guidance, ELEGANT is a world-wide joint R&D project involving several partners, combining different point tools.

2.2 SPECIFY-EXPLORE-REFINE (SER)

The SER component provides system level design space exploration and model refinement. Starting from an abstraction specification of the desired functionality written in SpecC, SER allows interactive platform definition and specification mapping. SER then automatically implements the specification on the platform and generates various transaction-level models (TLMs) of the design. The SER engine has been developed by the Center for Embedded Computer Systems (CECS) at University of California, Irvine as a derivate of CECS' original SpecC-based System-On-Chip Environment (SCE) [4], where SER has been adapted to JAXA requirements and databases have been filled with necessary components for space and satellite applications.

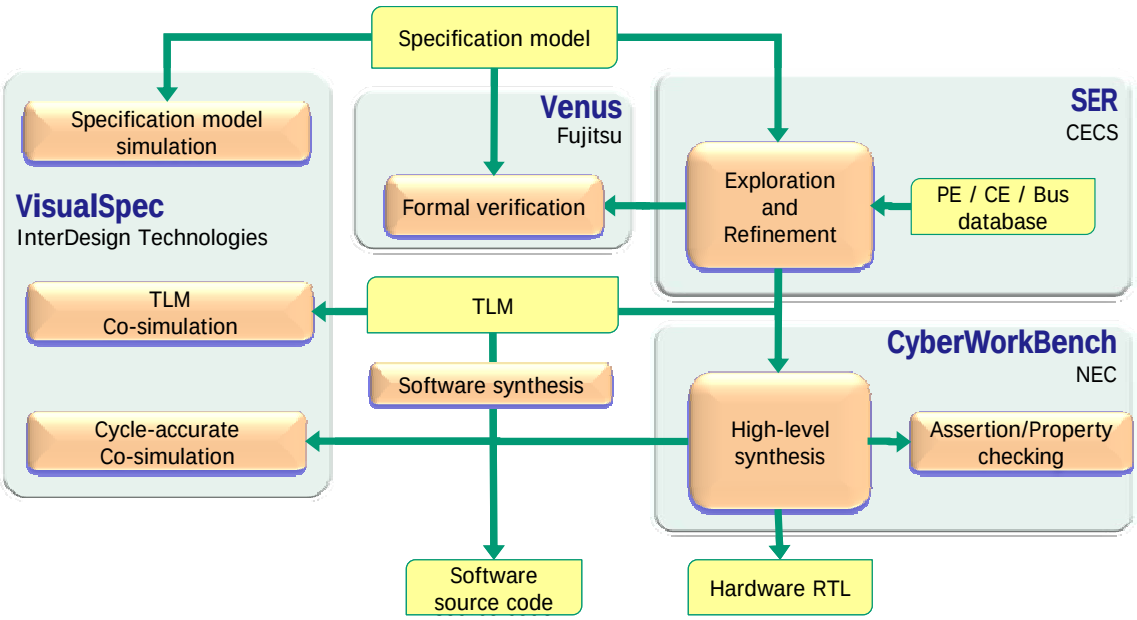


Figure 2: The ELEGANT environment

2.3 VISUALSPEC

In ELEGANT, models are captured and simulated using VisualSpec, a SpecC modeling and simulation environment supplied by InterDesign Technologies [6]. VisualSpec provides visualization and debugging support and optional integration of third-party instruction-set simulators (ISS) into the SpecC simulation backplane. VisualSpec supports profiling and estimation capabilities for model analysis and design quality feedback, including software execution time estimation and timing back-annotation of TLM software models using so-called FastVeri technology.

2.4 CYBERWORKBENCH

For synthesis of hardware components, ELEGANT includes the CyberWorkBench high-level, C-to-RTL synthesis tool originally developed at NEC [5].

As part of the ELEGANT project, Cyber has been adapted to accept SpecC input directly from the SER-generated models. Furthermore, it was extended to generate cycle-accurate (CA) SpecC models of the RTL output for co-simulation of the synthesized hardware with the rest of the system.

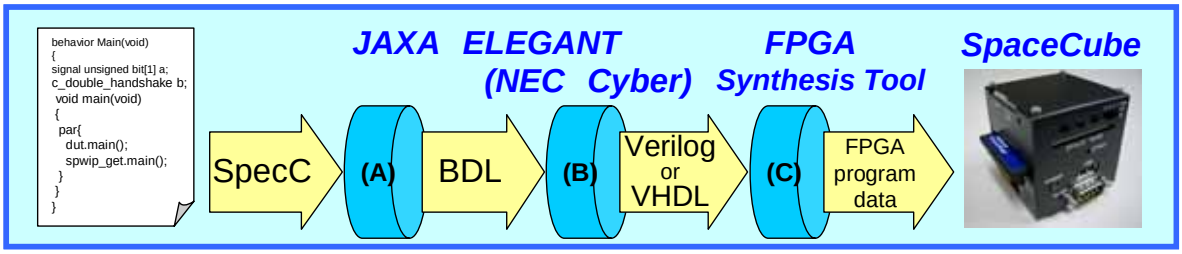
By designing hardware in C, software and hardware designers can communicate in the same language, which makes System LSI design more effective.

2.5 VENUS

ELEGANT contains a formal verification component, Venus, developed by Fujitsu Labs of America (FLA) and Tokyo University. Venus supports equivalence checking between different models in the ELEGANT design flow to guarantee correctness and model equivalence throughout the design process.

3 DESIGNING SPACE CUBE 2 WITH ELEGANT

JAXA initiated a project to evaluate ELEGANT design flow with the development of Space Cube 2. Using SER tools, hardware/software partitioning and exploration of the target architectures was performed. In the process, exploration was supported and driven by quantitative estimation (using VisualSpec estimation and profiling capabilities) to help select an appropriate implementation. Once a partitioning is selected, deriving FPGA data is a straight-forward process using CyberWorkBench as shown in figure 3.



(A) Program Conversion from SpecC to BDL (Behavioral Description Language)
(B) Behavioral Synthesis
(C) Logic Synthesis

Figure 3: FPGA implementation of RMAP from SpecC specification

The capacity of synthesized hardware on FPGAs or ASICs are slightly larger than ones which are logically synthesized from hand-coded HDL, and compact enough for space use.

4 REFERENCES

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