Critical SpaceWire Elements in RASTA

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INTRODUCTION

Many software and hardware components developed in European R&D activities <u>do not reach the required maturity level</u> for use in space projects, due to <u>lack of a representative environment</u> for validation and technology demonstration.

The RASTA (Reference Avionics System Testbench Activity) aims to fill this gap by providing a standard <u>hardware and software infrastructure</u> to integrate results from European activities (i.e. ESA activities).

OBJECTIVES

The RASTA objectives are:

- to allow new technology to <u>be validated and demonstrated</u> in a flight representative environment,

- to support mission and spacecraft design,

- to support on-board software verification and validation through the <u>project life-cycle</u> by means of a coherent emulations platform,

- to maximize <u>reuse of the existing avionics</u> technologies and to be scalable and flexible.

CONCEPT

- RASTA development platform is today based on the Compact PCI (cPCI) bus.

- Baseline communication between boards is performed via the PCI bus in the backplane.

- For other protocols, such as SpaceWire and Mil-Std-1553B, connectors are provided on the front-panel of each interface board.

- Current trend is to use less the PCI and more the SpaceWire interfaces on the front-panels.

- Future RASTA systems will probably use SpaceWire backplanes.

RASTA COMPACT PCI CRATE

RASTA is based on standard size 3U and 6U Compact PCI crates.

RASTA COMPACT PCI CRATE

Small size 3U Compact PCI crate

RASTA DEVELOPMENT BOARDS

The RASTA development system comprises processor and interface boards aimed at the development of avionics.

A variety of compact PCI boards are provided in a number of variations:

- Processors: LEON2/3, UT699, AT697, AT7913

- Serial links: SpaceWire/RMAP, Mil-Std-1553, CAN bus, Ethernet, USB, CCSDS TM/TC

- Peripherals: PCI, UART, JTAG, GPIO

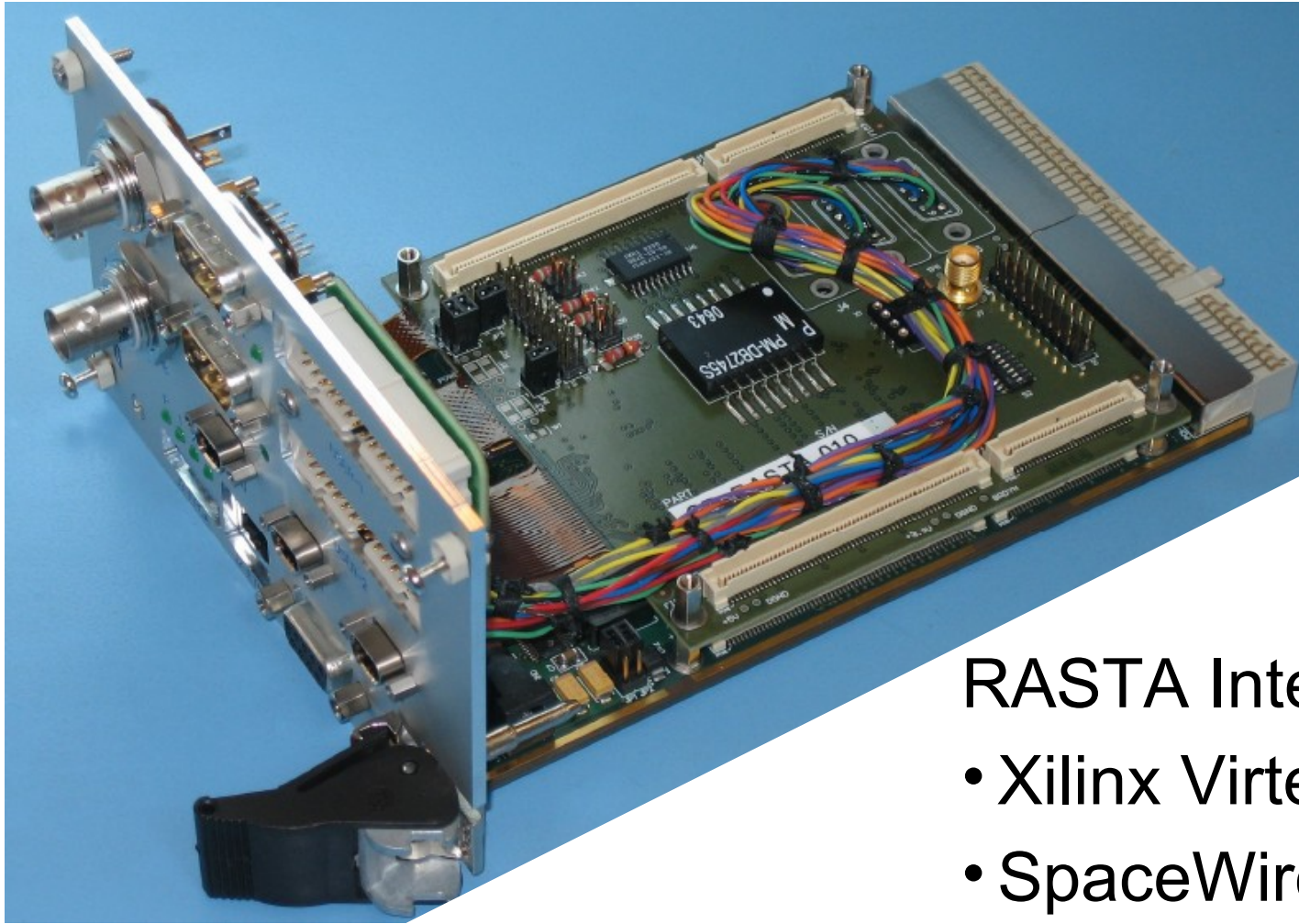- Memories: SRAM, SDRAM, FLASH PROM

SPACEWIRE IP CORE

Many of the RASTA boards are using the Aeroflex Gaisler SpaceWire IP codec, GRSPW.

The GRSPW codec implements an AMBA interface with DMA and RMAP in hardware.

The codec is optimised for system-on-a-chip integration, fault tolerant, portable, and available.
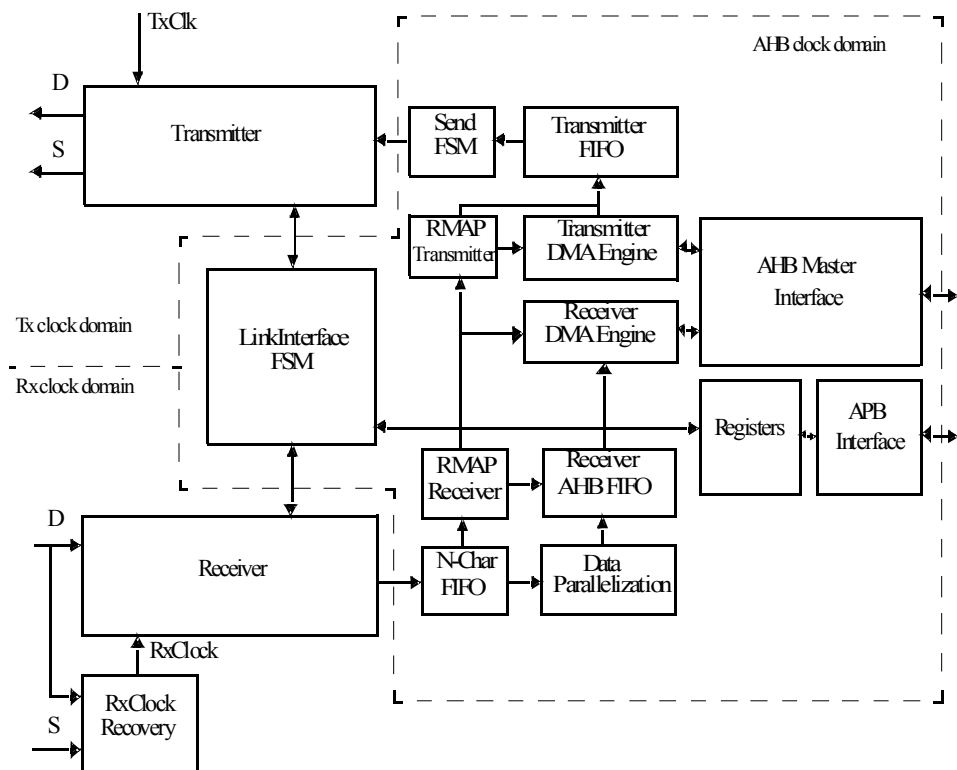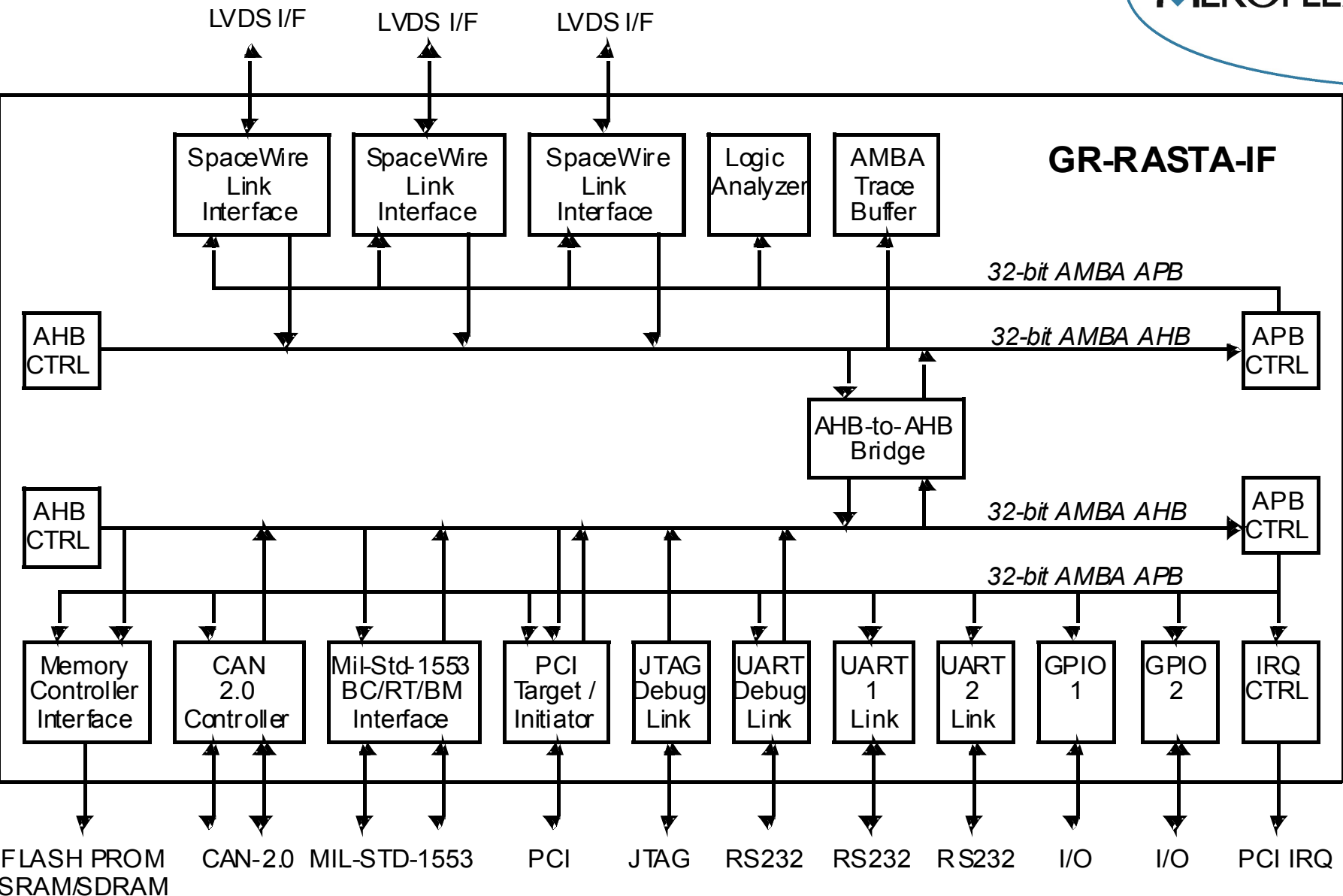
RASTA INTERFACE BOARD

RASTA Interface Board:

- Xilinx Virtex-4 FPGA
- SpaceWire
- CAN
- MIL-STD-1553B

AEROFLEX

AEROFLEX
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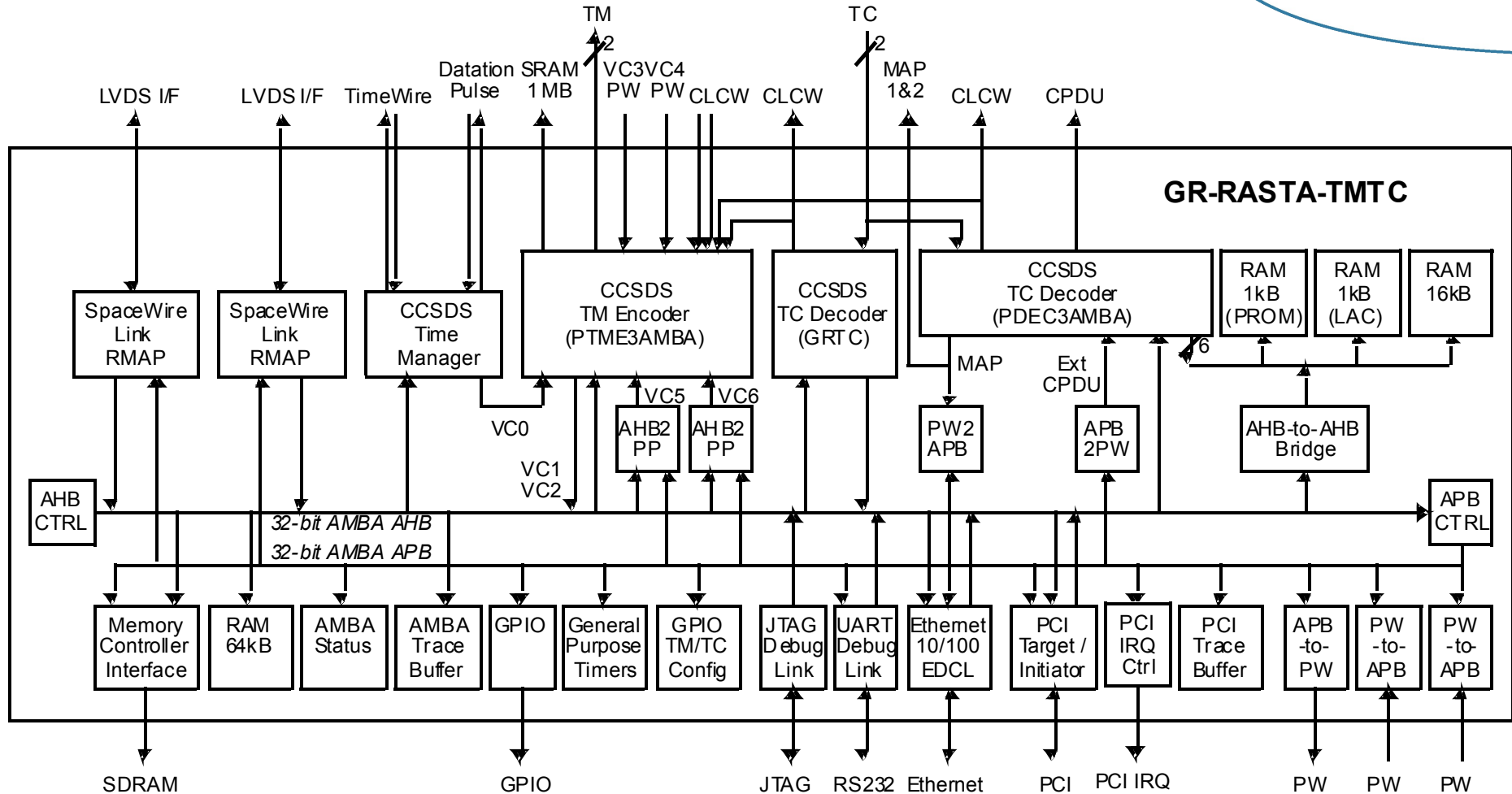
INTERNAL ARCHITECTURE

TELEMETRY & TELECOMMAND

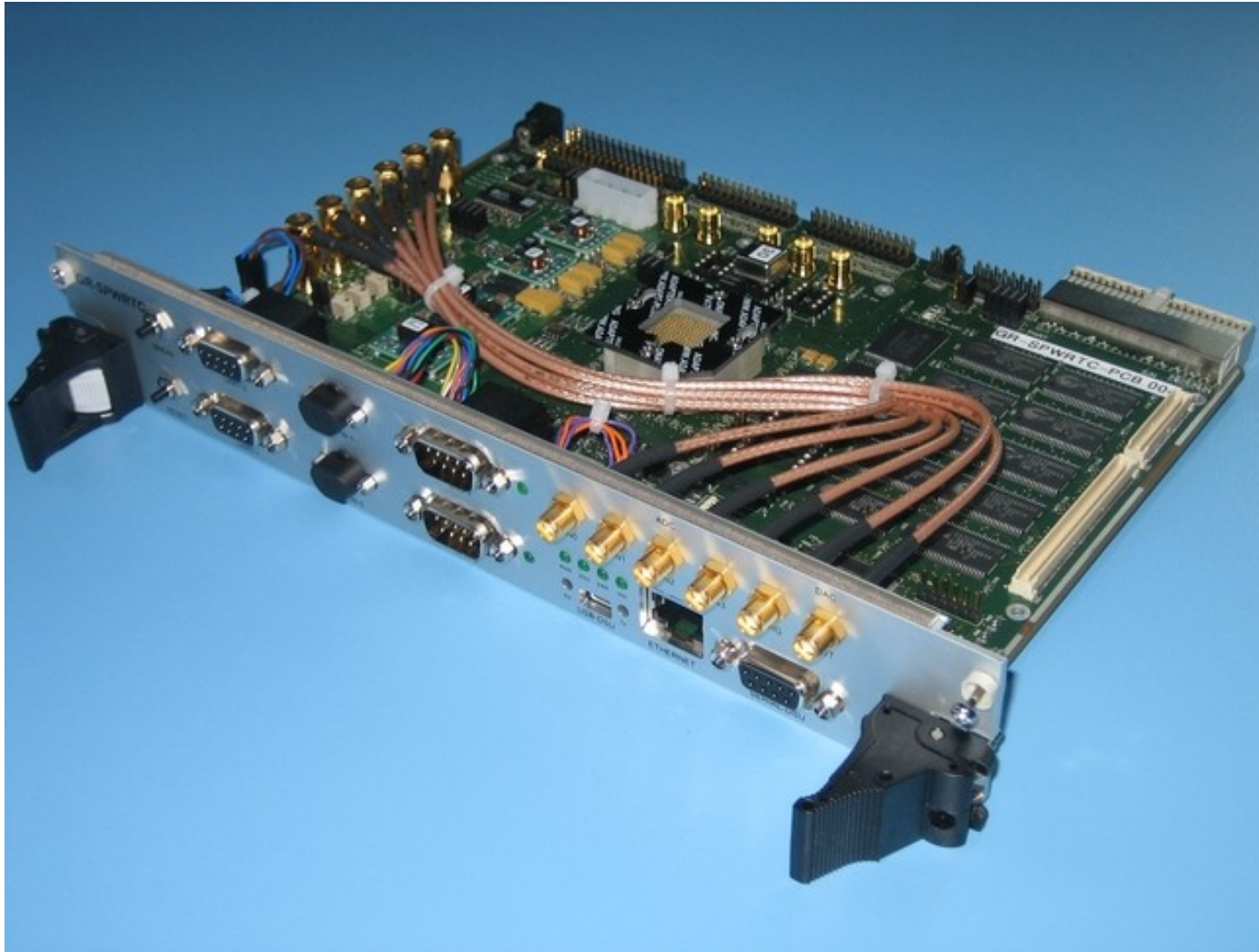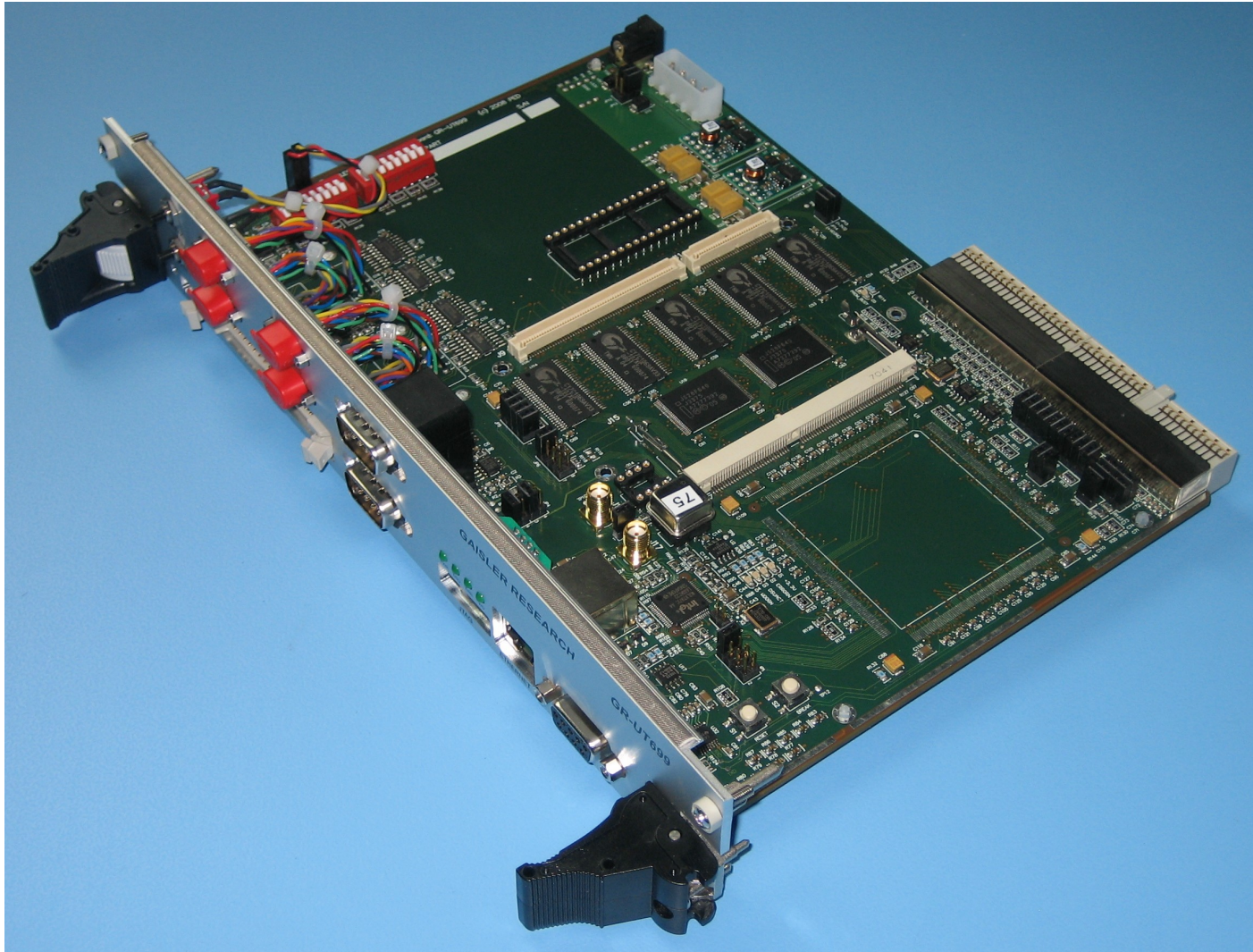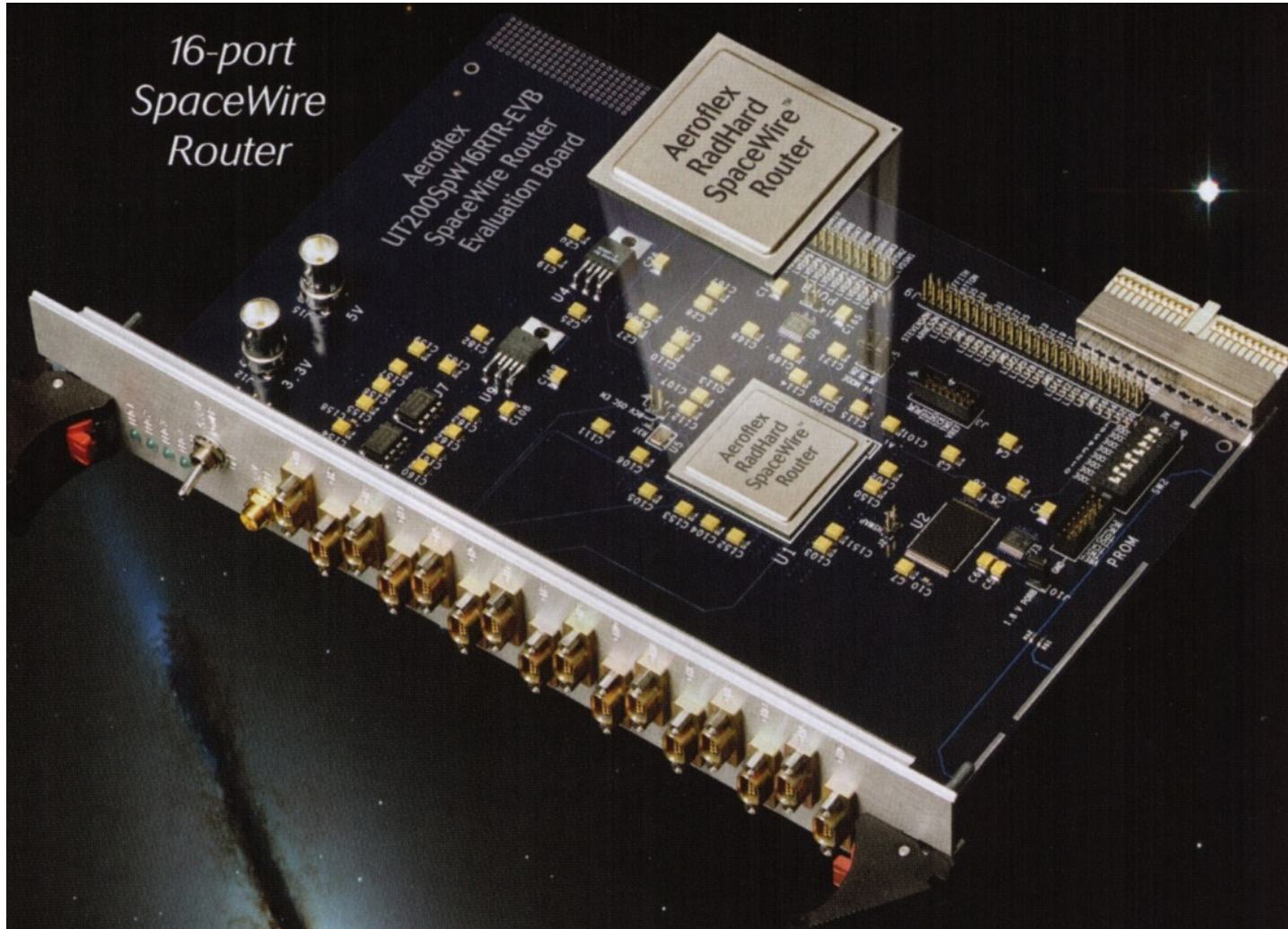# INTERNAL ARCHITECTURE

GR-CPCI-AT7913E BOARD

GR-CPCI-UT699 BOARD

SPACEWIRE ROUTER BOARDS

CONCLUSIONS

The RASTA initiative provides:

- A rich set of hardware ready for integration
- A rich set of IP cores ready for integration:
    - 32-bit SPARC fault-tolerant processor
    - SpaceWire codec with RMAP, etc.
- A platform to which new hardware elements can be easily added, both as IP cores and boards
- Ready-made software drivers for all hardware elements and IP cores
- A complete software environment